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DESIGNING COMPUTER CIRCUITS WITH A COMPUTER

By

Gene H. Leichner

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Digital computer circuits require that a number of tolerance conditions be met at one time. The number of these tolerance conditions which must be simultaneously satisfied in some circuits, such as a flipflop using transistor switching elements, is very large. The design of these circuits can be materially aided by using a digital computing machine to solve the resulting simultaneous equations. This paper discusses the derivation and solution of the five simultaneous non-linear algebraic equations resulting from an analysis of a flipflop circuit using transistors. The method has been carried out using the Illiac at the University of Illinois.

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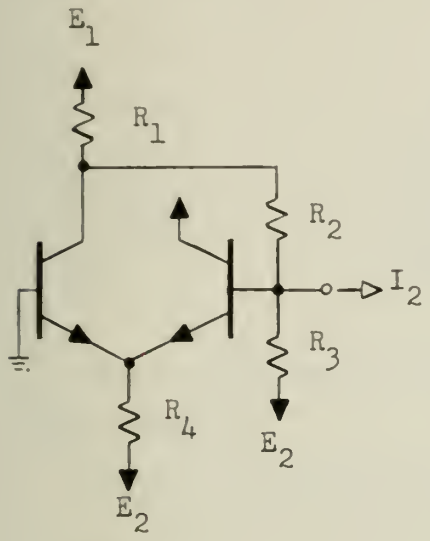
The circuit to be considered is that of a transistor flipflop as shown in Figure 1. All polarities are chosen for NPN transistors. In this analysis, the transistor r_e, r_b, and r_c will be assumed negligible for simplicity. It will also be assumed that $i_c = \alpha i_e$ and $i_b = (1-\alpha)i_e$ where α is the current gain of the transistor.



The given requirements are:

A	Power supply voltage tolerance
B	Resistor tolerance
E_2	Negative supply voltage (nominal)
I_2	Maximum current to be taken from output terminal
I_a	Maximum allowed collector current
V_a	Smallest acceptable negative output signal voltage
V_b	Smallest acceptable positive output signal voltage
V_c	Maximum allowed collector voltage
V_d	Minimum allowed collector voltage (To prevent saturation)
W	Maximum allowed collector dissipation
X	Maximum transistor current gain
Y	Minimum transistor current gain

The values required are:

E_1	Nominal positive supply voltage
I_1	Minimum collector current to be determined by R_4
R_1, R_2, R_3	Nominal values for the three resistors

The four conditions from which the equations will be written are shown in Figure 2 together with all the circuit values which would tend to violate the given conditions.

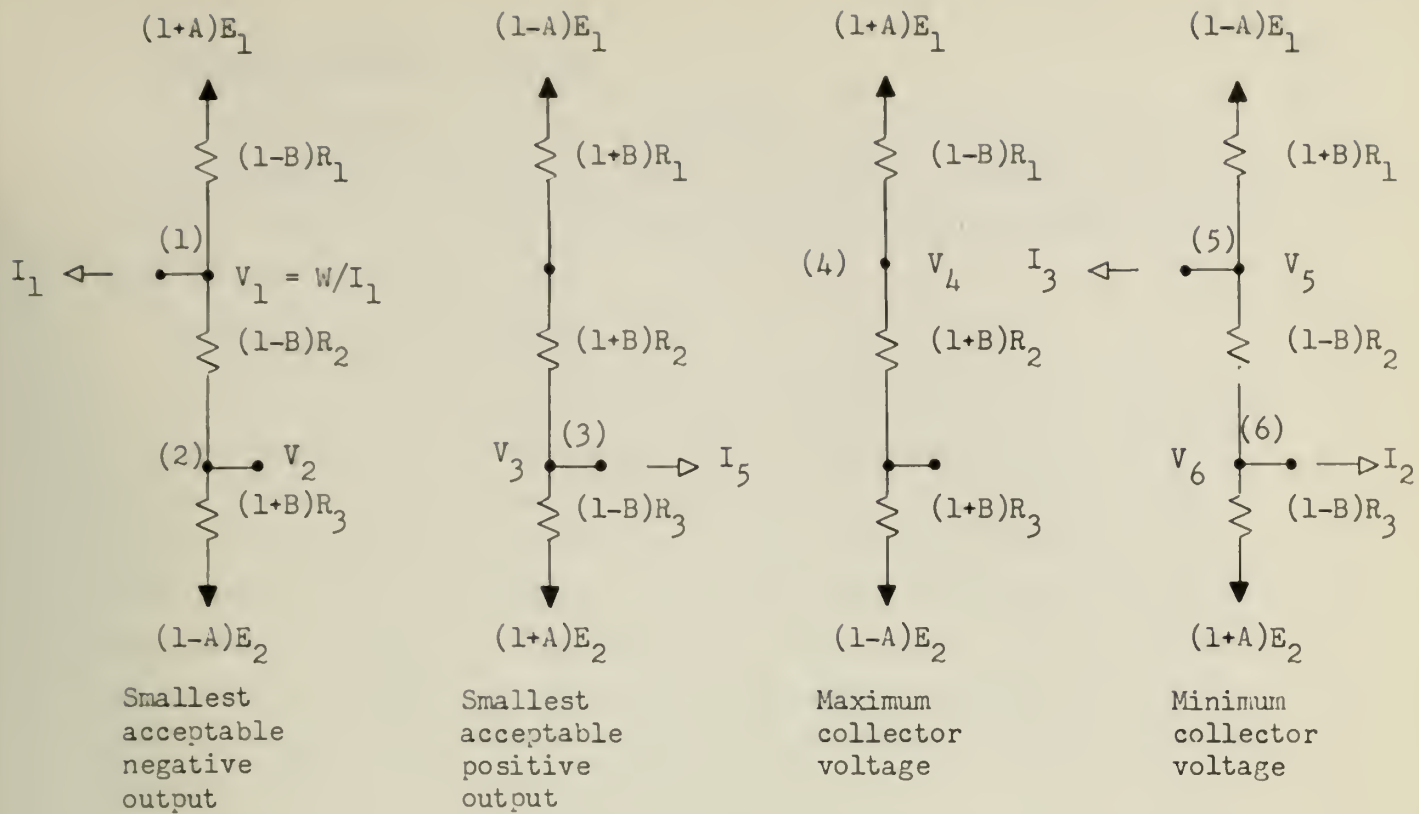


Figure 2.

The considerations involved in the four conditions will be discussed briefly.

Smallest acceptable negative signal output.

Aside from choosing the supply voltage and resistor tolerances in unfavorable directions, the collector current of the transistor has been chosen as the minimum value I_1, i.e. that which would result from $\alpha = Y$, a large value of R_4, and a small E_2. In addition, this is the condition requiring the greatest power dissipation from the transistor so V_1 has been expressed as a function of W and I_1.

Smallest acceptable positive signal output.

Again the most unfavorable directions for resistor and supply voltage tolerances have been chosen. Also the largest current, I_5, from the output terminal has been chosen. I_5 is the load current, I_2, plus the largest base current drawn by the emitter follower part of the flipflop, i.e. $\alpha = Y$, small R_4, and large E_2.

Maximum collector voltage.

In this case the transistor is assumed to be completely cut off, and the current I_5 which would normally be present is assumed to be zero, i.e. $\alpha = 1$ and $I_2 = 0$. The resistor and supply voltage tolerances also have been appropriately chosen.

Minimum collector voltage.

All the conditions which would cause the collector of the transistor to go most negative are represented here. The largest output current I_2 and the largest collector current are used, i.e. $\alpha = X$, small R_4, and large E_2. The emitter follower is cut off so its base current is zero. When a gate circuit is attached to the collector, its current and tolerances must be included in this condition. If it is of a type in which the current is essentially determined by an emitter resistor, as in the flipflop proper, the collector current of the flipflop can be doubled to include the gate. This is not shown here.

The circuit is described by writing the node equations at the marked nodes.

Node (1) $$\frac{W/I_1 - (1+A)E_1}{(1-B)R_1} + I_1 + \frac{W/I_1 - V_2}{(1-B)R_2} = 0$$

Node (2) $$\frac{V_2 - W/I_1}{(1-B)R_2} + \frac{V_2 - (1-A)E_2}{(1+B)R_3} = 0$$

Node (3) $$\frac{V_3 - (1-A)E_1}{(1+B)(R_1+R_2)} + I_5 + \frac{V_3 - (1+A)E_2}{(1-B)R_3} = 0$$

Node (4) $$\frac{V_4 - (1+A)E_1}{(1-B)R_1} + \frac{V_4 - (1-A)E_2}{(1+B)(R_2+R_3)} = 0$$

Node (5) $$\frac{V_5 - (1-A)E_1}{(1+B)R_1} + I_3 + \frac{V_5 - V_6}{(1-B)R_2} = 0$$

Node (6) $$\frac{V_6 - V_5}{(1-B)R_2} + I_2 + \frac{V_6 - (1+A)E_2}{(1-B)R_3} = 0$$

(7) $$I_3 = \left(\frac{X}{Y}\right)\left(\frac{1+B}{1-B}\right)\left(\frac{1+A}{1-A}\right) I_1$$

(8) $$I_5 = \left(\frac{1-Y}{Y}\right)\left(\frac{1+B}{1-B}\right)\left(\frac{1+A}{1-A}\right) I_1 + I_2$$

Equations (8) and (7) are to be substituted in (3) and (5) respectively. Equations (5) and (6) may be combined to eliminate V_6. Five simultaneous non-linear equations in E_1, I_1, R_1, R_2, and R_3 result. Note that the base current used by the emitter follower portion of the flipflop has been included in the analysis as part of I_5. This is necessary because the design is quite sensitive to I_5.

It is clear that the given specifications may be contradictory so that no solution exists. This is because several of the specifications place restrictions on the same quantities. Even if a solution exists, it is quite possible that some requirement will be more than just met. Therefore, it is not possible to do a brute force simultaneous solution of the five equations.

In order to solve the five equations obtained above, a program was prepared for a digital computer, Illiac. Note that the values for V_c, V_d, and I_a, in the specifications are limiting values so V_4, V_5, and I_4 will not necessarily be equal to them. The code was prepared, however, to operate the transistor at the specified maximum collector dissipation, W, to obtain the lowest possible circuit impedance. This should give the maximum speed of operation for a given transistor. Also, the V_a and V_b requirements will be just met, so in the worst tolerance cases the output voltages V_2 and V_3 will be equal to these values. If so desired, different choices as to which conditions are to be just met could be made.

The organization of the code for Illiac is as follows:

1. Read the specifications from a tape.

2. Set E_1 to the largest value to be considered.

3. Set $I_1 = I_a$, the largest permitted. So far a maximum gain network has been assured.

4. Solve equations (1), (2), and (3) for R_1, R_2, and R_3. No solution exists if one or more of these is negative or complex the first time, with largest E_1 and I_1.

5. Set $I_1 = I_2$, a value which is certain not to work, and repeat Step 4.

6. Continue to converge on the smallest value of I_1 for which a solution in Step 4 exists by a binary chop procedure. That is, at each step try I_1 halfway between the last value which worked and the highest value which did not work.

7. Check the saturation condition by equations (5) and (6). No solution exists if this condition is not met the first time since the network has maximum gain and the collector current has been reduced as far as possible.

8. Set $E_1 = V_b$, a value which is certain not to work, and repeat Steps 4 through 7. If there is no solution at Step 4 the first time, skip to Step 9.

9. Continue to converge on the smallest value of E_1 for which there is a solution in Step 4 and for which the saturation condition is met. Use a binary chop procedure as in Step 6.

10. Check the maximum collector voltage condition by equation (4). No solution exists if this condition is not met since the collector supply voltage is now as small as possible and the network gain has been reduced as far as possible.

The code used on the Illiac prints the given requirements and the conditions which are not met, followed by the values of E_1, I_1, R_1, R_2, R_3, V_4, and V_5 so the designer can see by how far the conditions were not met and perhaps make some changes in the specifications to make a solution possible. In case all the conditions were more than just met, he may be able to increase the tolerances to permit the use of less precise components.

Gene H. Leichner